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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/630,883	08/02/2000	Khosrow Golshan	82259/156	7954

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EXAMINER	
CHANG, AUDREY Y	
ART UNIT	PAPER NUMBER
2872	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	09/630,883	GOLSHAN, KHOSROW	
	Examiner	Art Unit	
	Audrey Y. Chang	2872	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-30 and 47-78* is/are pending in the application.

4a) Of the above claim(s) *23-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on **December 29, 2005** has been entered.

2. This Office Action is also in response to applicant's amendment filed on **October 31, 2005,** which has been entered into the file.

3. By this amendment, the applicant has amended claims 47, 55, 65 and 69.

4. **Claims 23-30 are withdrawn** from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 4.

5. Claims 47-78 remain pending in this application.

6. The rejections to claims under 35 USC 112, first paragraph, concerning added new matters set forth in the previous Office Action are withdrawn in response to the amendment.

Drawings

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "720" and "705" have both been used to designate the same element in Figure 8. No explicitly distinction is presented in the Figure. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application

must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The applicant is respectfully noted that even though the characters may be explained in the specification to refer to different elements, the drawings are still required to make the distinction between the two. Figure 8 still shows that the same element being designated by both characters "705" and "720".

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. **Claims 55-64 are rejected under 35 U.S.C. 112, first paragraph**, as containing subject matter which was not described in the specification in such a way as to **enable** one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 55 has been amended to include the phrase "a predetermined axis in the interference region along which maximum interference of optical signals in the interference region is caused".

The specification and claims fail to teach how could the maximum interference be **caused** "along a predetermined *axis* in the interference region". The applicant is respectfully requested to study the standard optic textbook for "interference". It is not clear how could the interference be caused along an axis. It is possible to define a direction along such the constructive interference occurs.

Claims 56-64 inherit the rejection from their based claim.

10. **Claims 68 and 77 are rejected under 35 U.S.C. 112, first paragraph,** as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification and the claims also fail to teach how could the optical logic circuit provides **both the NOT and NOT AND** logical functions, as recited in claims 68 and 77. The applicant is respectfully noted that page 6 of specification only discloses that the NOT AND (NAND) gate is used to **construct** a NOT gate. The specification does not give positive support for the logic function to be **BOTH** the NOT and NOT AND gates.

The applicant is advised to amend the claims to make the intended limitations clear. Applicant is respectfully noted as indicated by the applicant in the remark, no single interference region is possible to provide both the NOT and NAND functions. Claims 68 and 77 both recite a single Boolean logic function CONFIGURED of NOT gates and NOT AND (NAND) gates.

Claim Objections

11. Claims 47-78 are objected to because of the following informalities:

(1). The newly amended phrase "the periphery being a single, outer periphery" recited in the amended claims 47, 55, 65 and 69 is confusing and indefinite for it is not clear what does this "single" mean ? Judging form Figure 8, each of the interference regions has outer periphery made up of two parts, (element 760 and element 705). How do these two elements being considered as single periphery?

Appropriate correction is required.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 47-58, and 63-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Usagawa et al (PN. 5,233,205).

Usagawa et al teaches an *optical logic circuit* based on quantum well design wherein the optical logic circuit comprises a *substrate* comprising a *first optical material*, (such as 50 in Figure 5A or 95 in Figure 6A or 6B), and *a second optical layer overlaying the substrate* wherein the second optical layer are formed or patterned to have a plurality of *optical pathways* or *optical conduits*, (52 in Figure 5A or 100, 101 and 102 in Figure 6B), wherein an *interference regions* are formed of the second optical layer as shown in Figures 1A to 1G. Usagawa et al teaches that a plurality of *waveguides* (3, 4, and 5) are used to provide *optical input signals* to a plurality of *input gates* (10, 10' and 10"), wherein the optical input signals *enter* and *intercepts* at a three-dimensional region surrounded and *defined* by potential barriers (1), which then serves as the *interference region*, that includes or is connected to at least one *output window* (300') such that the input optical signals intercept and interfere with each other. An *output gate* (20, Figures 1A to 1G) is connected with the interference region to provide an *optical output signal*. Usagawa et al teaches that the optical output signal is a *Boolean logic output signal*, wherein the optical logic circuit can be designed to provide NOT (invert, Figure 1D), NOT AND (NAND, Figure 1F), and exclusive OR (NOR Figure 1G) optical logic functions, respectively.

Claims 47, 55, 65 and 69 have been amended to include the feature having the interference region comprises the second materials and is bounded on its periphery by material other than the second

material and the periphery being a single, outer periphery such that only the interference region is within the periphery. This feature is not clearly supported by the specification and is objected for the reasons stated above. **Usagawa** et al teaches explicitly that the interference region is the region defined by the optical pathways or conduits (52, or 101-109), that optical signals pass through and interfere with each other. Usagawa et al teaches *explicitly* that the optical pathways or optical conduits or the interference region comprises the second material such as GaAs and the interference region is bounded at its periphery (such as barrier 2, 2' and 1 in Figures 1A-3E and 51 in Figure 5A, please see columns 5 and 11) by a material such as $Al_xGa_{1-x}As$, which is different from the GaAs material for making up the interference region. As shown in Figure 5A of Usagawa et al the periphery that surrounds the interference region (52) is a **single outer periphery** the same way as the instant application shows in Figure 8. With regard to the amended claim 65, the second material GaAs is optical transmission material.

With regard to the feature that the "output signal having one of two intensities, either a substantially on or a substantially off intensity". This feature is implicitly met by the disclosure of Usagawa et al, since Usagawa et al teaches a *Boolean logic gate and* the optical output signal is a *Boolean logic output signal,* which implicitly include ON and OFF output intensities.

With regard to claims 48, 51, 56-58, 66, 70-72, and 74, Usagawa et al teaches the optical logic circuit may be designed to give NOT logic function as the output signal, (Figure 1D), wherein an optical input signal may be a *constant coherent input signal*, ("1") that enters the interference regions through the input gate (10), and a *second input coherent optical signal* (X) may be switched ON or OFF and enters the interference region through the *second input gate* (10'). When the second coherent input signal is turned ON, the input signals from both gates interfere with each other to essentially cancel each other so that an invert or NOT optical logical function is resulted as the optical output signal, (please see Figure 1D, column 8, lines 8-25).

With regard to claims 49-50, 67, 68, 69, 75, and 77, Usagawa et al teaches that the optical logic circuit may be designed to give NAND logic function, (Figure 1F), wherein three input optical signals are used. One skilled in the art certainly can design the optical processor to comprise various logic gates for the desired logical functions and purposes.

This reference has met all the limitations of the claims. With regard to the feature concerning "*the output is positioned along a chosen line, of many lines, along which destructive interference occurs*". Usagawa et al does not teach such explicitly however this feature is to the least inherently met by the cited reference **since** the optical logic gate of Usagawa et al *performs the same Boolean logic functions* as the instant application and the output signal of the Boolean logic function is the *direct result of the interference* of the input optical signals, the arrangement of the output therefore has to align in the claimed manner to produce the Boolean logic output results. With regard to the feature of the "interference line is aligned with the output when the light input at the second input is on". This feature is implicitly included in the disclosure since only when light propagates through the pathways, the quantum waves are generated. It is implicitly true that within the interference region there is at least one axis along which maximum constructive interference would occur.

With regard to claim 69, it is implicitly true that the interference properties of the input signals in the interference region are determined by the input signals and the physical structure of the interference region.

With regard to claims 63 and 64, this reference also does not teach explicitly that a laser diode or a semiconductor diode is used as the light source for generating the optical wave. However laser diode or laser semi-conductive diode are both well known light sources for operating optical logic circuit, such feature is either inherently met or an obvious modification to one skilled in the art for providing proper light sources with proper energy required to operate the optical logic circuit.

14. Claims 59-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Usagawa et al as applied to claim 55 above, and further in view of the patent issued to Logan et al (PN. 3,837,728).

The optical logic circuit taught by **Usagawa** et al as described for claim 55 above has met all the limitations of the claims. Usagawa et al teaches that the optical logic circuit may use gallium arsenide (GaAs) material as the substrate layer however it does not teach explicitly to use doped GaAs material, silicon or doped silicon materials as the substrate layer and optical layer for pathways (i.e. waveguides) respectively. However these materials are all well known semi-conductive materials for making waveguides or even optical logic circuit, as demonstrated by the teachings of Logan et al wherein a GaAs layer is used as substrate layer wherein doped GaAs layer is used as the optical waveguide. It would then have been obvious matters of design choices to one skilled in the art to use the claimed materials as the materials for designing the optical logic circuits for the benefit of using desired materials that provide the desired performance. It has also been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended used as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Response to Arguments

15. Applicant's arguments filed on October 31, 2005 have been fully considered but they are not persuasive. The newly amended claims have been fully considered and they are rejected for reasons stated above.

16. Applicant's arguments are mainly regard to the newly amended features and they have been fully addressed in the paragraphs above. Applicant is respectfully noted that Usagawa et al teaches explicitly that the barriers (1) and barriers (2) are made of the same material, (please see column 5, lines 30-35). The cited Usagawa et al reference therefore meets the claim limitations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Audrey Y. Chang whose telephone number is 571-272-2309. The examiner can normally be reached on Monday-Friday (8:00-4:30), alternative Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Dunn can be reached on 571-272-2312. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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